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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,015	03/31/2004	Darren Slawecki	42P17273	9217

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/815,015	SLAWECKI, DARREN	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-32* is/are allowed.

6)☒ Claim(s) *1-7,11,14-18,21 and 33* is/are rejected.

7)☒ Claim(s) *8-10,12,13,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 7/07/2005 has been reviewed and considered with the following results:

As to the objection to claim 2, Applicant's amendments and clarifications have overcome the objection, as such; the objection has been withdrawn.

As to the rejection to claims 21 and 28, under 35 U.S.C. 112, 2nd paragraph, Applicant's clarifications have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to the claims made in the previous Office Action mailed on 6/14/2005 are now withdrawn in view of Applicant's amendments. However, Applicant's amendments necessitate new grounds of rejection as set forth below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (US 6,404,258; previously cited).

With regard to claim 1, Ooishi discloses in Figs. 10-38 a delay circuit, comprising a first circuit (IVa) including a circuit input to receive a reference signal (DIN); a circuit output to output a delayed signal (103) being a delayed response to the reference signal; a logic circuit

(100b-100c of IVa) including a logic input and a logic output, the logic input coupled to the circuit input to generate an inversion of the reference signal at the logic output; a pull up path (102a) coupled to the logic output; and a pull down path(102b) coupled to the logic output; a falling edge delay circuit coupled to the pull up path to control delay of a falling edge of the reference signal; and a rising edge delay circuit coupled to the pull down path to control delay of a rising edge of the reference signal.

With regard to claim 2, the first circuit comprises an enable circuit (IVb) and wherein the logic circuit further includes an enable input to receive an enable signal (VP, VN) for enabling the delay circuit.

With regard to claims 3-7, the reference also meets the recited limitations in these claims.

With regard to claim 11, Ooishi discloses in Figs. 10-38 a delay circuit, comprising an inverting enable circuit (by given the broadest reasonable interpretation; circuit IVa is the inverting enable circuit because the circuit is enabled by the signals VP &VN) including a circuit input to receive a reference signal (DIN) and a circuit output to output a delayed signal (103) being a delayed inversion of the reference signal; a falling edge delay circuit coupled to the inverting enable circuit to control delay of a falling edge of the reference signal; and a rising edge delay circuit coupled to the inverting enable circuit to control delay of a rising edge of the reference signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14-18, 21, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi in view of Fletcher et al. (US 6,928,572).

With regard to claims 14, Ooishi discloses in Figs. 10-38 a circuit, comprising a clock enable circuit including a clock input to receive a reference clock signal (DIN); a circuit output (103) to output a delayed clock signal being a delayed response to the reference clock signal; and an inverter circuit (IVb); a falling edge delay circuit (PR0, PR1, PR2) coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and a rising edge delay circuit (NR0, NR1, NR2) coupled to the enable circuit to control delay of a rising edge of the reference clock signal. The circuit of Ooishi meets all of the claimed limitations except for a NAND logic circuit (L1 in instant Fig. 3) having a first NAND input coupled to receive the reference clock signal, a second NAND input coupled to the enable input, and a NAND output. Fletcher et al. teaches in Fig. 2 a circuit having a NAND logic circuit as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the NAND logic circuit taught by Fletcher et al. in Fig. 38 of Ooishi in order to control the activation/de-activation of the enable circuit using the enabling control signal.

With regard to claims 15-18, the reference also meets the recited limitations in these claims.

With regard to claim 21, given that the references shows the precise structure claimed by the present invention and that the claim 21 add nothing to the claimed structure of the circuit, the

phenomena, whether it be use in hardware behavioral code, register transfer level code, a netlist, or a circuit layout, is an intended use of the structure and does not carry patentable weight. Therefore, as the claimed structure is met by the prior art, the intended use of the circuit is likewise met. Recall that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987.)

With regard to claim 33, the above discussed circuit of the references meets all of the claimed limitations except for an inverter (L10 in instant Fig. 5) coupled between the clock input and the first NAND input. In other word, that inverter is implemented on signal path. However, it is well known in the art for circuit designers to implement the inverter on signal path for inverting the logic level of the output signal, as the inverters 37-40 shown in Fig. 10 of Ooishi. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the inverter in the signal path in the circuit of the prior art for the expected advantage of being able to provide the desired logic level to subsequent circuit, which are in each case optimally matched to its application.

Allowable Subject Matter

6. Claims 22-32 are allowed.

7. Claims 8-10, 12, 13, 19, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a delay circuit (300 in instant Fig. 3), as recited in claim 8, having specific structural limitation such as the enable circuit further includes an inverter coupling the logic output to the circuit output and wherein the logic circuit comprises a NAND logic gate including first and second NAND inputs and a NAND output, the first NAND input corresponding to the logic input, the second NAND input corresponding to the enable input, and the NAND output corresponding to the logic output, the pull up path includes a first transistor to selectively couple the NAND output to the falling edge delay circuit, the pull down path includes second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a delay circuit (300 in instant Fig. 3), as recited in claim 12, having specific structural limitation such as the inverting enable circuit further comprises: a NAND logic gate having first and second NAND inputs and a NAND output, the second NAND input coupled to the enable input; a first inverter coupling the circuit input to the first NAND input; a pull up path including a first transistor to selectively couple the NAND output to the rising edge delay circuit; a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the falling, edge delay circuit; and an second inverter coupling the NAND output to the circuit output, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Claim 19 is allowed for similar reasons; note the above discussion with regard to claim 12.

The prior art of record fails to disclose or fairly suggest an integrated circuit (700 in instant Fig. 7), as recited in claim 22, comprising a clock distribution network to distribute a reference clock signal throughout the integrated circuit; and having specific structural limitation such as each of clock delay circuits comprising a clock enable circuit including: a clock input to receive the reference clock signal; an enable input; a circuit output to output a delayed clock signal being a delayed response to the reference clock signal; a NAND logic circuit having a first NAND input coupled to receive the reference clock signal, a second NAND input coughed to the enable input and a NAND output; and an inverter circuit coupling the NAND output to the circuit output a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal; latches each clocked according to the delayed clock signal output from each of the clock delay circuits; and logic clusters to compute logic values, the latches coupled to buffer the logic values between clock edges of the delayed clock signals, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
October 1, 2005

TIMOTHY P. CALLAHAN
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